IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

KURT P. WACHTLER ET AL.

Serial No. 09/788,075 (TI-17462.2)

Filed February 16, 2001

For: HDI LAND GRID ARRAY PACKAGED DEVICE
HAVING ELECTRICAL AND OPTICAL INTERCONNECTS

Art Unit 2827

Examiner Luan C. Thai

Commissioner for Patents
Washington, D. C. 20231

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1 to 5 and 7 to 25, all of the rejected claims. Claim 6 has been allowed. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after final rejection.

SUMMARY OF INVENTION

ISSUES

The issues on appeal are as follows:

1. Whether claims 1, 23 and 24 are anticipated by Maruyama et al. (U.S. 4,199,777) under 35 U.S.C. 102(b).

2. Whether claims 1, 5, 8 to 17 and 21 to 25 are patentable over Marcinkiewicz et al. (U.S. 5,422,513) under 35 U.S.C. 103(a).

3. Whether claims 2, 3 and 18 to 20 are patentable over Marcinkiewicz et al. in view of Nakabu et al. (U.S. 4,544,989) under 35 U.S.C. 103(a).

4. Whether claim 4 is patentable over Marcinkiewicz et al. in view of Eichelberger (U.S. 5,144,747) under 35 U.S.C. 103(a).

5. Whether claim 7 is patentable over Marcinkiewicz et al. in view of Cole et al. (U.S. 5,338,975) under 35 U.S.C. 103(a).

GROUPING OF CLAIMS

The claims do not stand or fall together for reasons set forth hereinbelow under ARGUMENT.

ARGUMENT

ISSUE 1

Claims 1, 23 and 24 were rejected under 35 U.S.C. 102(b) as being anticipated by Maruyama et al. (U.S. 4,199,777). The rejection is without merit.

Claim 1 requires, among other features, "a thin film overlay electrically connecting bond pads on said semiconductor device to electrically conductive pads on a layer of said thin film overlay facing away from said semiconductor device". No such structure is taught or even remotely suggested by Maruyama et al. either alone or in the combination as claimed. Note that the claim requires that the thin film overlay provide the electrical connection between the bond pads on the semiconductor device to electrically conductive pads on the thin film overlay. Maruyama et al. has no such structure. In Fig. 2 of Maruyama et al. the terminal 4 extends through the silicon dioxide layer 6 with the silicon dioxide layer making no electrical connection as required by claim 1. The same reasoning is applied to Figs. 4 and 6 of Maruyama et al. since the layers 12 and 24 are merely of a different material.

Claims 23 and 24 depend from claim 1 and therefore define patentably over Maruyama et al. for at least the reasons presented above with reference to claim 1.

In addition, claim 23 further limits claim 1 by requiring at least one additional semiconductor device in the package. No such combination is taught or suggested by Maruyama et al.

Claim 24 further limits claim 23 by requiring that the thin film overlay connect bond pads on the semiconductor devices to electrically conductive pads on a layer of the thin film overlay facing away from the semiconductor device. No such combination is taught or suggested by Maruyama et al.

ISSUE 2

Claims 1, 5, 8 to 17 and 21 to 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Marcinkiewicz et al. (U.S. 5,422, 513). The rejection is without merit.

As demonstrated by the Declaration of Ronald O. Neerings, Esq., the attorney who initially prepared this application, the invention as described and claimed herein was conceived with due diligence from a date prior to the effective filing date of Marcinkiewicz et al.up to the filing date of the parent of the subject application. Accordingly, Marcinkiewicz et al. is not available as a reference in this application. It is readily apparent that the Declaration of Mr. Neerings establishes conception with diligence up to filing of the parent of the subject application prior to the effective filing date of Marcinkiewicz et al.

ISSUE 3

Claims 2, 3 and 18 to 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Marcinkiewicz et al. in view of Nakabu et al (U.S. 4,544,989). The rejection is without merit for the reason stated above as to Marcinkiewicz et al.

ISSUE 4

Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Marcinkiewicz et al. in view of Eichelberger (U.S. 5,144,747). The rejection is without merit for the reason stated above as to Marcinkiewicz et al.

ISSUE 5

Claim 7 was rejected under 35 U.S.C. 103(a) as being unpatentable over Marcinkiewicz et al. in view of Cole et al. (U.S. 5,338,975). The rejection is without merit for the reason stated above as to Marcinkiewicz et al.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

1. A device comprising:

a package having a cavity therein;

a semiconductor device in said cavity, said semiconductor device having at least one optical receiver and/or transmitter adjacent a surface of said semiconductor device facing away from said package; and

a thin film overlay electrically connecting bond pads on said semiconductor device to electrically conductive pads on a layer of said thin film overlay facing away from said semiconductor device.

2. The device of Claim 1, including an electrically conductive medium on said electrically conductive pads for connecting said device directly to external hardware.

3. The device of Claim 2, in which the dimensions of said cavity match or oxceed the dimensions of the semiconductor device.

4. The device of Claim 3, wherein said package includes at least one heat slug.

5. The device of Claim 1, wherein said thin film overlay includes a hole between said optical receiver and/or transmitter on said semiconductor device and said layer of said thin film overlay facing away from said semiconductor device.

7. The device of Claim 2, including a device attach adhesive in the cavity.

8. The device of Claim 1, wherein said thin film overlay includes at least one layer of dielectric material and at least one layer of conductive material.

9. The device of Claim 8, wherein a layer of thin film overlay adjacent said semiconductor device is a layer of dielectric material.

10. The device of Claim 9, 2h343in said layer of conductive material is patterned into a first layer of respective conductors.

11. The device of Claim 10, wherein some of said respective conductors are pads and some are planes.

12. The device of Claim 11, including vias filled with electrically conductive material from bond pads of said semiconductor device through said layer of dielectric material and to said respective conductors.

13. The device of Claim 12, including a second lay er of dielectric material adjacent said first layer of respective conductors and a second layer of conductive material patterned into a second layer of respective conductors.

14. The device of Claim 13, including vias filled with electrically conductive material from conductors of said first layer of respective conductors, through said second layer of said dielectric material, and to conductors of said second layer of respective conductors.

15. The device of Claim 14, wherein said additional conductor of said second layer of respective conductors are patterned into an array of pads.

16. The device of Claim 12, including at least one additional alternating pair of layers of dielectric material and conductive material patterned into a layer of respective conductors, with each additional layer of dielectric layer being adjacent the previous layer of respective conductors.

17. The device of Claim 16, including vias filled with electrically conductive material from conductors of a previous layer of respective conductors, through an adjacent layer of dielectric material and to conductors of another layer of respective conductors.

18. The device of Claim 17, including solder balls attached to the last layer of respective conductors.

19. The device of Claim 17, including metal bumps attached to the last layer of respective conductors.

20. The device of Claim 17, including polymer connectors attached to the last layer of respective conductors.

21. The device of Claim 8, including at least a second dielectric layer between said dielectric layer and said layer of conductive material.

22. The device of Claim 16, including at least an additional dielectric layer between each dielectric layer and the next layer of conductive material.

23. The device of Claim 1, including at least one additional semiconductor device within said package.

24. The device of Claim 23, wherein said thin film overlay connects bond pads on said semiconductor devices to electrically conductive pads on a layer of said thin film overlay facing a way from said semiconductor device.

25. The device of Claim 24, wherein said thin film overlay connects some of the bond pads of said semiconductor devices to each other and other of the bond pads to electrically conductive pads on a layer of said thin film overlay facing away from said semiconductor devices.